Application Note 3111
Interfacing the DS3144 Framer with the DS3154 LIU

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INTRODUCTION

This application note contains the information necessary to interface between the DS3144, a quad-port DS3/E3 framer, and the DS3154, a quad-port DS3/E3/STS-1 line interface unit (LIU).

The DS3144 has four independent DS3/E3 framers on a single die and includes all necessary circuitry to frame and format four separate DS3 or E3 channels. Each framer in this device is independently configurable to support M23 DS3, DS3 C-Bit Parity, or G.751 frame formats with all applicable alarm detection and generation. The DS3144 interfaces to a variety of LIUs, microprocessor buses, and other system components without glue logic. The digital-data interface to the LIU can be binary (NRZ) or bipolar (POS/NEG), and provides internal B3ZS/HDB3 encoders and decoders.

The DS3154 quad LIU performs the functions necessary for interfacing at the physical layer to DS3, E3, or STS-1 lines. Each LIU has an independent receive and transmit path and a built-in jitter attenuator. Each port of the DS3154 is independently configurable. The DS3154 has either hardware or CPU bus configuration options.

This application note also applies to the following Dallas Semiconductor framers with Dallas Semiconductor LIUs:

DS3/E3 FRAMER	DESCRIPTION
DS3141	Single-Port Framer
DS3142	Dual-Port Framer
DS3143	Triple-Port Framer
DS3146	6-Port Framer
DS3148	8-Port Framer
DS31412	12-Port Framer

DS3/E3/STS-1 LIU	DESCRIPTION
DS3151	Single-Port LIU
DS3152	Dual-Port LIU
DS3153	Triple-Port LIU

DS3144 RECEIVE-FRAMER LIU-INTERFACE PINS

Receive Positive Data Input/Receive NRZ Data Input (RPOS/RNRZ): If BIN = 0 in the MC1 register, the LIU interface is in bipolar (POS/NEG) mode. In this mode, the framer clocks in the serial data stream in AMI format. RPOS = 1 from an external LIU indicates a positive pulse was received on the line; RNEG = 1 from the LIU indicates a negative pulse was received on the line. If BIN = 1, the framer is in binary (NRZ) LIU-interface mode. In this mode the framer clocks in the serial data stream in binary format on the RNRZ pin. RNRZ = 1 indicates a 1 in the data stream; RNRZ = 0 indicates a 0 in the data stream.

Receive Negative Data Input/Receive Line-Code Violation Input (RNEG/RLCV): If BIN = 0 in the MC1 register, the LIU interface is in bipolar (POS/NEG) mode. In this mode, the framer clocks in the serial data stream in alternate-mark inversion (AMI) format. RPOS = 1 from an external LIU indicates a positive pulse was received on the line, while RNEG = 1 from the LIU indicates a negative pulse was received on the line. If BIN = 1, the framer is in binary (NRZ) LIU interface mode. In this mode the framer clocks in the serial data stream in binary format on the RNRZ pin and line-code violations on the RLCV pin.

Receive Clock Input (RCLK): RCLK is used to clock data into the receive framer on RPOS/RNEG (bipolar LIU interface mode) or RNRZ (binary LIU interface mode). If RCLKI = 0 in the MC5 register, data is clocked into the framer on the rising edge of RCLK. If RCLKI = 1, data is clocked in on the falling edge of RCLK. RCLK is normally accurate to within ±20ppm when sourced from an LIU, but the framer can also accept a gapped clock up to 52MHz on RCLK, such as those commonly soured from ICs that map/demap DS3 and E3 to/from SONET/SDH.

DS3144 TRANSMIT-FORMATTER LIU-INTERFACE PINS

Transmit Positive Data Output/Transmit NRZ Data Output (TPOS/TNRZ): If BIN = 0 in the MC1 register, the LIU interface is in bipolar (POS/NEG) mode. In this mode, the transmit formatter outputs the serial data stream in AMI format. TPOS = 1 signals an external LIU to drive a positive pulse on the line, while TNEG = 1 tells the LIU to drive a negative pulse on the line. If BIN = 1, the LIU interface is in binary (NRZ) mode. In this mode, the transmit formatter outputs the serial data stream in binary format on the TNRZ pin. TNRZ = 1 indicates a 1 in the data stream, while TNRZ = 0 indicates a 0.

Transmit Negative Data Output (TNEG): If BIN = 0 in the MC1 register, the LIU interface is in bipolar (POS/NEG) mode. In this mode, the transmit formatter outputs the serial data stream in AMI format. TPOS = 1 signals an external LIU to drive a positive pulse on the line, while TNEG = 1 tells the LIU to drive a negative pulse on the line. If BIN = 1, the LIU interface is in binary (NRZ) mode. In this mode the transmit formatter outputs the serial data stream in binary format on the TNRZ pin, and TNEG is driven low.

Transmit Clock Output (TCLK): TCLK is used to clock data out of the transmit formatter on TPOS/TNEG (bipolar LIU interface mode) or TNRZ (binary LIU interface mode). If TCLKI = 0 in the MC5 register, data is clocked out of the formatter on the rising edge of TCLK. If TCLKI = 1, data is clocked out on the falling edge of TCLK. TCLK is normally a buffered (and optionally inverted) version of TICLK. When either line loopback or payload loopback is active, TCLK is a buffered (and optionally inverted) version of RCLK. When a clock is not present on TICLK and MC1:LOTCMC = 1, TCLK is a buffered (and optionally inverted) version of RCLK.

DS3154 RECEIVE-LIU FRAMER-INTERFACE PINS

Receiver Positive AMI/Receiver Data (RPOS/RDAT): When the receiver is configured to have a bipolar interface (RBIN = 0), RPOS pulses high for each positive AMI pulse received. When the receiver is configured to have a binary interface (RBIN = 1), RDAT outputs decoded binary data. RPOS/RDAT is updated either on the falling edge of RCLK (RCINV = 0) or the rising edge of RCLK (RCINV = 1).

Receiver Negative AMI/Line-Code Violation (RNEG/RLCV): When the receiver is configured to have a bipolar interface (RBIN = 0), RNEG pulses high for each negative AMI pulse received. When the receiver is configured to have a binary interface (RBIN = 1), RLCV pulses high to flag code violations. RNEG/RLCV is updated either on the falling edge of RCLK (RCINV = 0) or the rising edge of RCLK (RCINV = 1).

Receiver Clock (RCLK): The recovered clock is output on the RCLK pin. Recovered data is output on the RPOS/RDAT and RNEG/RLCV pins on the falling edge of RCLK (RCINV = 0) or the rising edge of RCLK (RCINV = 1). During a loss of signal (RLOS = 0), the RCLK output signal is derived from the LIU's master clock.

DS3154 TRANSMIT-LIU FRAMER-INTERFACE PINS

Transmitter Positive AMI/Transmitter Data (TPOS/TDAT): When the transmitter is configured to have a bipolar interface (TBIN = 0), a positive pulse is transmitted on the line when TPOS is high. When the transmitter is configured to have a binary interface (TBIN = 1), the data on TDAT is transmitted after B3ZS or HDB3 encoding. TPOS/TDAT is sampled either on the rising edge of TCLK (TCINV = 0) or on the falling edge of TCLK (TCINV = 1).

Transmitter Negative AMI (TNEG): When the transmitter is configured to have a bipolar interface (TBIN = 0), a negative pulse is transmitted on the line when TNEG is high. When the transmitter is configured to have a binary interface (TBIN = 1), TNEG is ignored and should be wired either high or low. TNEG is sampled either on the rising edge of TCLK (TCINV = 0) or on the falling edge of TCLK (TCINV = 1).

Transmitter Clock (TCLK): A DS3 (44.736MHz _20ppm), E3 (34.368MHz _20ppm), or STS-1 (51.840MHz _20ppm) clock should be applied at this signal. Data to be transmitted is clocked into the device at TPOS/TDAT and TNEG either on the rising edge of TCLK (TCINV = 0) or the falling edge of TCLK (TCINV = 1).

REGISTERS OF THE DS3144 AND THE DS3154 REQUIRED FOR THE INTERFACE:

Table 1 shows the DS3144 registers that are responsible for top-level configuration, control, and status of each framer, including resets, clocks, pin controls, and line-interface functions.

Table 1. Line Interface Register Map for DS3144

ADDR.	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
01h	MC1	LOTCMC	ZCSD	BIN	MECU	AECU	TUA1	DISABLE	RST
02h	MC2	OSTCS	TCCLK	N/A	N/A	N/A	DLB	LLB	PLB
03h	MC3	TDENMS	TSOFC	TOHENI	TOHI	TSOFI	TICLKI	TDATI	TDENI
04h	MC4	RDENMS	ROOFI	RLOSI	RDATH	RSOFI	ROCLKI	RDATI	RDENI
05h	MC5	RNEGI	RPOSI	RCLKI	TNEGH	TPOSH	TNEGI	TPOSI	TCLKI
06h	ISR1	N/A	N/A	N/A	N/A	INT4	INT3	INT2	INT1
08h	MSR	LORC	LOTC	T3E3	FEAC	HDLC	BERT	COVF	N/A
09h	MSRL	LORCL	LOTCL	N/A	N/A	N/A	N/A	COVFL	OSTL
0Ah	MSRIE	LORCIE	LOTCIE	T3E3IE	FEACIE	HDLCIE	BERTIE	COVFIE	OSTIE

Note: *Bits that are underlined are read-only bits. Bits that are marked N/A are undefined. Undefined bits are reserved for future enhancements and must always be written with logic 0 and ignored when read.*

Table 2 shows the DS3144 DS3/E3 framer registers. In this register map, underlined bits are for read-only. Bits that are marked N/A are undefined. Undefined bits are reserved for future enhancements and must always be written with logic 0 and ignored when read.

These registers in Table 2 are responsible for top-level configuration, control, and status of each framer on DS3 and E3 mode.

Table 2. DS3/E3 Framer Register Map for DS3144

ADDR	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
10	T3E3CR1	E3SnC1	E3SnC0	T3IDLE	TRAI	TAIS	TPT	CBEN	DS3M
11	T3E3CR2	FRESYNC	N/A	TFEBE	AFEBED	ECC	FECC1	FECC0	E3CVE
12	T3E3EIC	MEIMS	FBEIC1	FBEIC0	FBEI	T3CPBEI	T3PBEI	EXZI	BPVI
18	T3E3SR	N/A	N/A	SEF	T3IDLE	RAI	AIS	OOF	LOS
19	T3E3SRL	COFAL	N/A	SEFL	T3IDLEL	RAIL	AISL	OOFL	LOSL
1A	T3E3SRIE	COFAIE	N/A	SEFIE	T3IDLEIE	RAIIE	AISIE	OOFIE	LOSIE
1B	T3E3IR	RUA1	T3AIC	E3Sn	N/A	EXZL	MBEL	FBEL	ZSCDL
20	BPVCR1	BPV7	BPV6	BPV5	BPV4	BPV3	BPV2	BPV1	BPV0
21	BPVCR2	BPV15	BPV14	BPV13	BPV12	BPV11	BPV10	BPV9	BPV8
22	EXZCR1	EXZ7	EXZ6	EXZ5	EXZ4	EXZ3	EXZ2	EXZ1	EXZ0
23	EXZCR2	EXZ15	EXZ14	EXZ13	EXZ12	EXZ11	EXZ10	EXZ9	EXZ8
24	FECR1	FE7	FE6	FE5	FE4	FE3	FE2	FE1	FE0
25	FECR2	FE15	FE14	FE13	FE12	FE11	FE10	FE9	FE8
26	PCR1	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
27	PCR2	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8
28	CPCR1	CPE7	CPE6	CPE5	CPE4	CPE3	CPE2	CPE1	CPE0
29	CPCR2	CPE15	CPE14	CPE13	CPE12	CPE11	CPE10	CPE9	CPE8
2A	FEBECR1	FEBE7	FEBE6	FEBE5	FEBE4	FEBE3	FEBE2	FEBE1	FEBE0
2B	FEBECR2	FEBE15	FEBE14	FEBE13	FEBE12	FEBE11	FEBE10	FEBE9	FEBE8

The DS3154 can operate in either hardware mode or CPU bus mode.

In hardware mode, pulling the input pins high or low does all configurations. All the status information is reported on status output pins. Internal registers are not accessible in hardware mode. The device is configured for hardware mode when the HW pin is wired high (HW = 1).

In CPU bus mode, most of the configuration and status pins used in hardware mode are reassigned to be address, data, and control lines that interface to an 8-bit microprocessor bus. The device is configured for CPU bus mode when the HW pin is wired low (HW = 0).

With the exception of the HW pin, configuration and status pins available in hardware mode have corresponding register bits in the CPU bus mode. The hardware mode pins and the CPU bus mode register bits have identical names and functions, with the exception that all register bits are active high. Table 3 shows the register map of DS3154, which can be used for the interface with DS3144.

Table 3. Register Map for DS3154

ADDR.	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	GCR1	E3M	STS	LLB	RLB	TDSA	TDSB	—	RST
01h	TCR1	—	TBIN	TCINV	TJA	TPD	TTS	TLBO	—
02h	RCR1	ITU	RBIN	RCINV	RJA	RPD	RTS	RMON	RCVUD
03h	SR1	—	—	TDM	PRBS	—	—	RLOL	RLOS
04h	SRL1	—	—	TDML	PRBSL	PBERL	RCVL	RLOLL	RLOSL
05h	SRIE1	—	—	TDMIE	PRBSIE	PBERIE	RCVIE	RLOLIE	RLOSIE
06h	RCVL1	RCV[7]	RCV[6]	RCV[5]	RCV[4]	RCV[3]	RCV[2]	RCV[1]	RCV[0]
07h	RCVH1	RCV[15]	RCV[14]	RCV[13]	RCV[12]	RCV[11]	RCV[10]	RCV[9]	RCV[8]
08h–0Fh	TEST	—	—	—	—	—	—	—	—

IMPLEMENTING THE INTERFACE BETWEEN THE FRAMER AND LIU

The DS3144 device will always have power-on reset enabled. After reset, all read/write control register bits are reset to 0 except for RDATH and TUA1, which are set to 1. Complete operation details for the reset of this device is available in the data sheet (www.maxim-ic.com/DS3144). The DS3144 needs to be configured for either DS3 or E3 after resetting the device. In all modes, the TUA1 bit in the MC1 register and RDATH bit in the MC4 register must be cleared. These bits are set to 1 at reset to generate an unframed all-ones (E3 AIS) signal on both the transmit LIU interface (TPOS/TNEG) and the receive system interface (RDAT).

After reset the default LIU interface format of DS3144 is bipolar (POS/NEG) with B3ZS/HDB3 encoding and decoding enabled. To change framer operation after reset to binary (NRZ) format with B3ZS/HDB3 encoding and decoding disabled (disabled in the framer but should be enabled in the LIU), BIN bit needs to be set to 1 in the MC1 register.

FRAMER INTERFACE FORMAT AND THE B3ZS/HDB3 DECODER FOR DS3154

The data can be output in either binary or bipolar format. To select the bipolar interface format, the RBIN pin needs to be low in hardware mode. In CPU bus mode, the RBIN configuration bit needs to be cleared.

In bipolar format, the B3ZS/HDB3 decoder is disabled and the recovered data is buffered and output on the RPOS and RNEG outputs. Received positive-polarity pulses are indicated by RPOS = 1, while negative-polarity pulses are indicated by RNEG = 1.

In bipolar interface format, the receiver simply passes on the received data and does not check it for BPV or EXZ occurrences. To select the binary interface format, the RBIN pin needs to be high in hardware mode. In CPU bus mode, the RBIN configuration bit needs to be set.

In binary format, the B3ZS/HBD3 decoder is enabled, and the recovered data is decoded and output as a binary value on the RDAT pin. Code violations are flagged on the RLCV pin.

To support interface to a variety of neighboring components, the polarity of RCLK can be inverted. Normally, data is output on the RPOS/RDAT and RNEG/RLCV pins on the falling edge of RCLK. To output data on these pins on the rising edge of RCLK, the RCINV pin needs to be pulled high in hardware mode or the RCINV configuration bit needs to be set in CPU bus mode.

The RCLK, RPOS/RDAT, and RNEG/RLCV pins can be tri-stated to support protection switching and redundant-LIU applications. This tri-stating capability supports system configurations where two or more LIUs are wire-ORed together and a system processor selects one to be active. To tri-state RCLK, RPOS/RDAT, and RNEG/RLCV, assert the RTS pin or the RTS configuration bit. Figure 1 shows the functional diagram for the Dallas Semiconductor Framer DS3144 and the Dallas Semiconductor LIU DS3154.

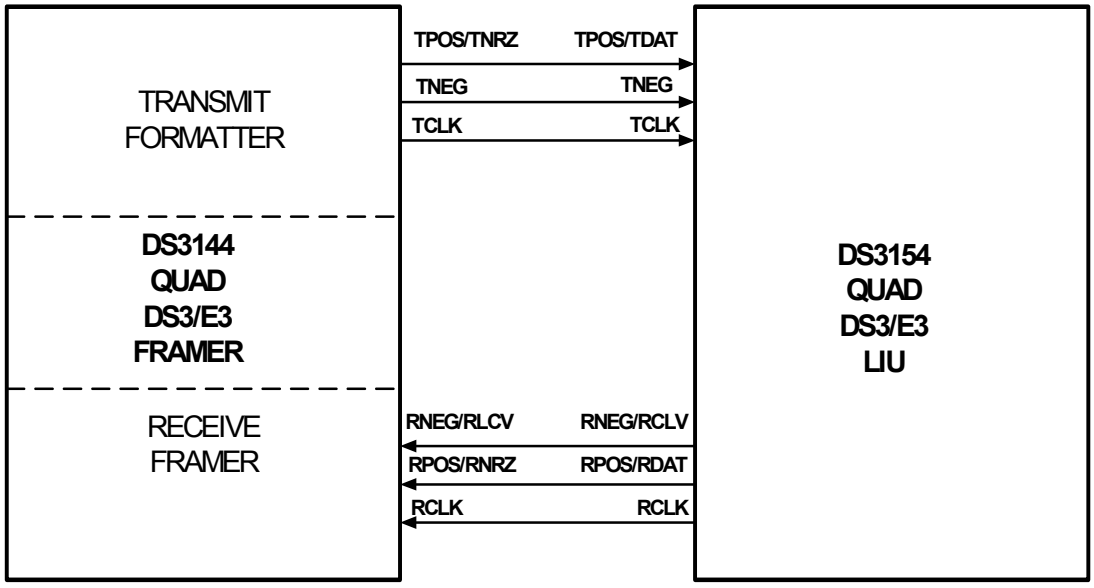

Figure 1. Functional Diagram for the Framer and LIU

CONCLUSION

For more help on designing the hardware for the interface between framer and LIU, refer to the DS3144DK data sheet, available online at www.maxim-ic.com/DS3144DK.

For further questions about the operations of and/or the interface between Dallas Semiconductor framers and LIUs, please contact the Dallas Semiconductor Telecommunications applications support team via email at telecom.support@dalsemi.com, or call 972-371-6555.